JEDEC STANDARD

Description of 1.8 V CMOS Logic Devices

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DESCRIPTION OF 1.8 V CMOS LOGIC DEVICES

(From JEDEC Board Ballot JCB-99-52, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Purpose

The purpose is to provide a standard specification for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

2 Scope

This standard defines dc interface, switching parameters and test loading for digital logic devices based on 1.8 V (nominal) power supply levels.

3 Definitions for the purpose of this document

Prefixes “54” or “74” immediately preceding family name indicate the operating temperature range. For example, 54xxx refers to the Military (MIL) version of devices which are specified over temperature range of –55 ºC to +125 ºC. 74xxx refers to the Commercial (COM’L) version of devices which are specified over –40 ºC to +85 ºC.

4 Standard specifications

4.1 Absolute maximum continuous ratings[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{DD}	dc Supply voltage		-0.5 to +2.5	V
V_{IN}	dc Input voltage		-0.5 to V_{DD} + 0.5	V
V_{OUT}	dc Output voltage	Output in OFF state	-0.5 to V_{DD} + 0.5	V
T_{STG}	Storage temperature		-65 to +150	ºC

NOTES

1 Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under these conditions is not implied.

2 Under transient conditions these ratings may be exceeded as defined elsewhere in this specification.

4 Standard specifications (cont'd)

4.2 Recommended operating conditions

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{DD}	dc supply voltage	1.65	1.95	V
V_{IN}	Input voltage	0	V_{DD}	V
V_{OUT}	Output voltage	0	V_{DD}	V
T_{AMB}	Operating free-air temperature	-40	+85	ºC

4.3 DC specifications

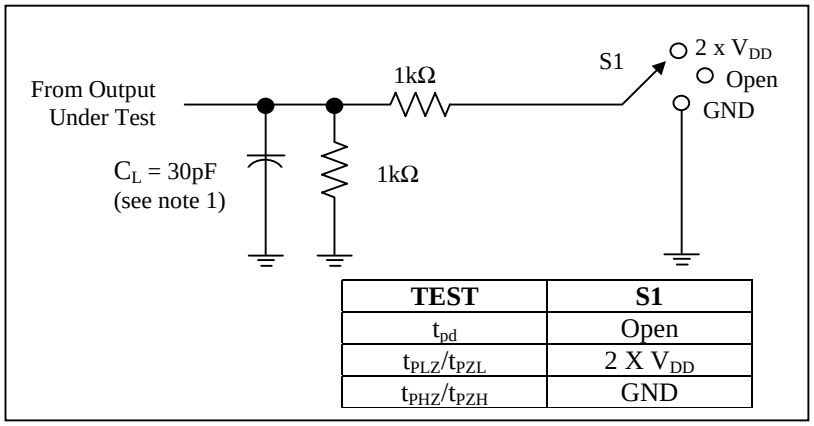
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			MIN	MAX	
V_{IH}	Input High Voltage		$0.65V_{DD}$	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3	$0.35V_{DD}$	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{DD} – 0.2		V
V_{OH}	Output High Voltage	I_{OH} = -2 mA	V_{DD} – 0.45		V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA		0.2	V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA		0.45	V

NOTES

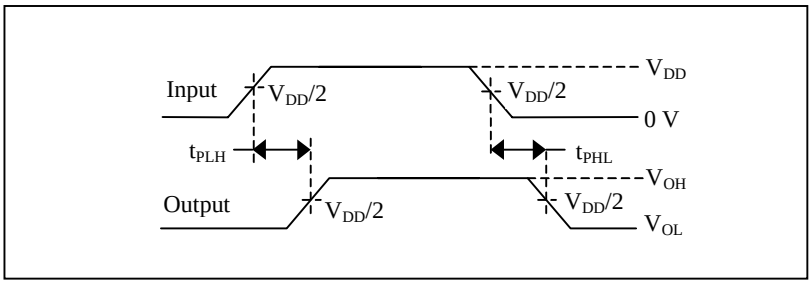
1 Over recommended operating conditions

2 Voltages are referenced to GND

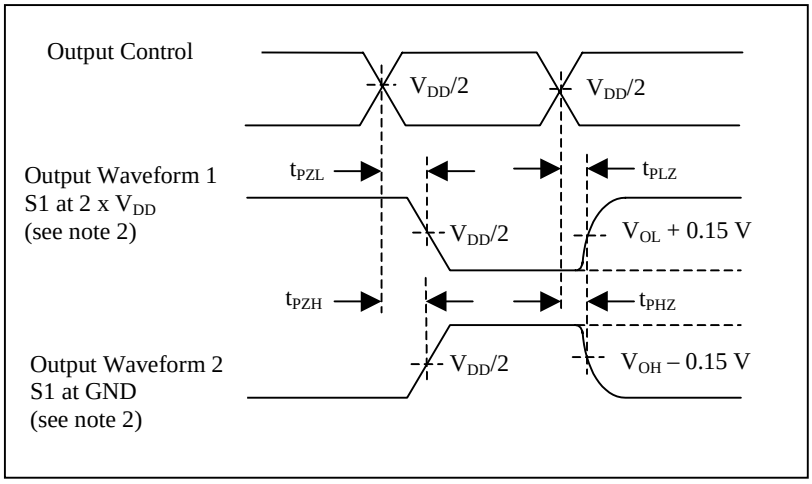
5 Test circuit and switching waveforms



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 X V_{DD}
t_{PHZ}/t_{PZH}	GND



Measurement 1 — Propagation delay times

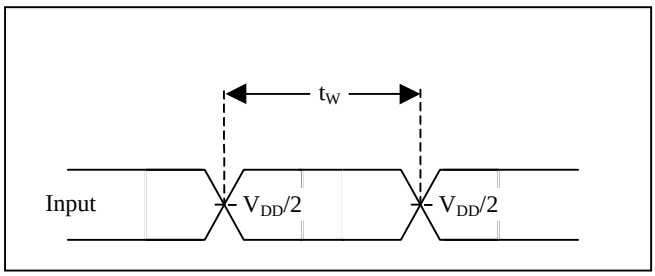


Measurement 2 — Enable and disable times

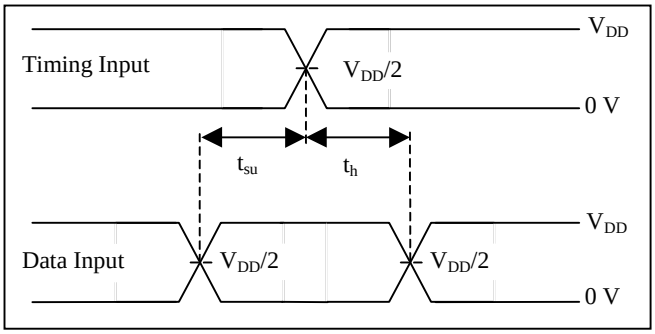
NOTES

1 C_L includes probe, and jig capacitance.
2 Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3 All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r = t_f \leq 2$ ns.
4 The outputs are measured one at a time with one transition per measurement.
5 t_{PLZ} and t_{PHZ} are the same as t_{dis}.
6 t_{PZL} and t_{PZH} are the same as t_{en}.
7 t_{PLH} and t_{PHL} are the same as t_{pd}.

5 Test circuit and switching waveforms (cont'd)



Measurement 3 — Pulse duration (width) measurements



Measurement 4 — Setup and hold times

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